FLASH MEMORY CELL AND FABRICATING METHOD THEREOF

DESCRIPTION

CROSS-REFERENCE TO RELATED APPLICATION

[Para 1] This application is a divisional application of U.S. application serial No. 10/604,861, filed on August 22, 2003, now U.S. Pat. No. 6,815,758

BACKGROUND OF THE INVENTION

[Para 2] Field of Invention

[Para 3] The present invention relates to a structure and method of fabricating a semiconductor device. More particularly, the present invention relates to a structure and method of fabricating a flash memory cell.

[Para 4] Description of Related Art

[Para 5] A typical flash memory cell includes a stacked structure of a control gate and a floating gate, and a source/drain region on two sides of the structure, where the control gate and the floating gate are generally constructed of polysilicon. In a conventional method of process of a flash memory cell, a positive high voltage is applied, in a programming mode, to a control gate to cause electrons injecting to a floating gate so that the channel under the floating gate is turned off in a reading operation; while a negative high voltage is applied, in an erasing mode, to the control gate to cause electrons ejecting from the floating gate so that the channel under the floating gate is turned on in a reading operation. Data in the memory cell are judged by whether the channel is turned on.

[Para 6] However, over-erase often occurs in a process to erase a flash memory cell. In other words, too much electrons eject from the floating gate